IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

SYNOPSYS, INC., a Delaware Corporation, Plaintiff and Counter-Defendant, v. MAGMA DESIGN AUTOMATION, a Delaware Corporation, Defendant and Counterclaimant. AND RELATED COUNTERCLAIMS.	C.A. No. 05-701 GMS

MAGMA DESIGN AUTOMATION'S OPENING MARKMAN BRIEF

Dated: November 3, 2006

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I. NATURE AND STAGE OF THE PROCEEDING

Synopsys, Inc. ("Synopsys") filed this action on September 26, 2005, alleging that Magma infringed U.S. Patents 6,434,733; 6,766,501; and 6,192,508 (the '733, '501, and '508 patents, respectively). [D.I. 1] On October 19, 2005, Magma Design Automation, Inc. ("Magma") answered, raising antitrust and unfair competition counterclaims based on Synopsys's alleged fraudulent procurement of the '733 and '501 patents and assertion of patents it knew to be invalid and unenforceable. [D.I. 5] Synopsys has since withdrawn the '733 and '501 patent allegations from this litigation and has dedicated the patents to the public, but Magma's antitrust and unfair competition claims relating to those patents remain.

Magma amended its answer and counterclaims shortly after it first answered, adding a charge of infringement of U.S. Patent No. 6,505,328 (the '328 patent) [D.I. 7] and, on May 31, 2006, by leave of the Court, it added charges of infringement of four additional U.S. Patents, No. 6,519,745; 6,857,116; 6,954,093; and 6,931,610 (the '745, '116, '093, and '610 patents respectively). [D.I. 76] Magma has since withdrawn the '610 patent from this litigation.

The parties have exchanged proposed claim constructions regarding the disputed terms of the patents at issue, and have met and conferred regarding those claim constructions. The parties' opening briefs on claim construction are due November 3, 2006, and their reply briefs on November 17, 2006. The claim construction hearing is scheduled for November 28, 2006.

II. INTRODUCTION

Magma accuses Synopsys of infringing four Magma patents. From an initial list of 52 terms to be construed in the Magma patents, the parties met and conferred and narrowed the disputed terms to be construed by the Court to three.

For the one remaining asserted Synopsys patent, the '508 patent, five terms are submitted for claim construction, as well as certain elements of the asserted means-plus-

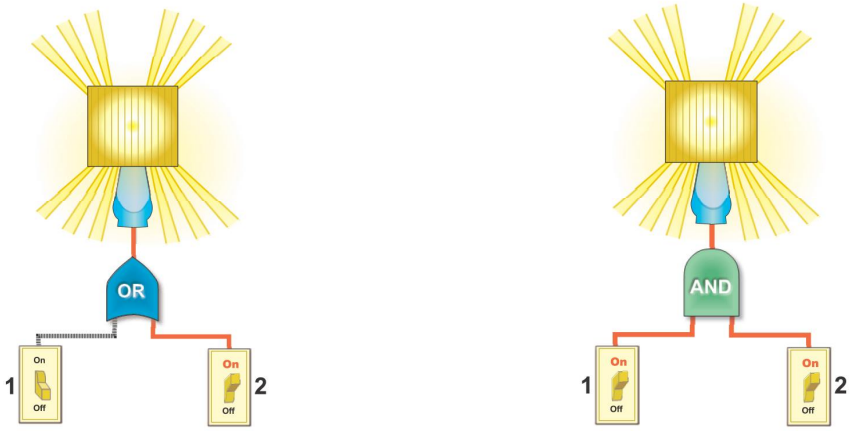
function claims. As will become clear from the argument below, the disproportionate number of claim terms to be construed in the '508 patent is a direct result of Synopsys's attempt to rewrite that patent to cover what Magma does.

III. ELECTRONIC DESIGN AUTOMATION (EDA) SOFTWARE

The design and layout of integrated circuits ("ICs," also known as computer "chips") were once done by hand but are now automated. Since the mid-1970's, electronic design automation ("EDA") software that converts the chip designer's high-level descriptions of how a circuit should operate into a physical layout has been used to design the circuit. The design process involves three basic phases or steps: (1) ***synthesis***, (2) ***placement*** and (3) ***routing***.

Synthesis is the translation of a high-level circuit description into basic logic functions. The high-level description is generally provided in a format known as a hardware description language (HDL), and it describes how the circuit will behave, but not how the circuit must be built to produce that behavior. By way of example, a room might have two light switches, one at each doorway, and a lamp. If a chip designer wants either switch to turn the lamp on, regardless of the setting of the other switch, the designer could write an HDL program to describe that behavior. Nothing in the HDL program would mandate what logic functions should be used to achieve that result.

During synthesis, EDA software converts the HDL description into a map of interconnected "cells." A "cell" performs a simple logic function, such as receiving two signals and producing a result. The cells are selected from a cell library containing a collection of standardized cells with various characteristics and functions. The logical functions "and," "or" and "not" are examples of cells, and in our light switch example, an "or" cell would allow either switch to turn on the lamp: if switch 1 **or** switch 2 is on, the lamp will be on. If the designer wanted the lamp to illuminate only when both switches were on, the designer could use an "and" cell: switch 1 **and** switch 2 cause electricity to flow to the lamp.



The result of synthesis is a data file known as a "netlist" that describes which cells will be used, and their interconnections. If, for instance, there were had five rooms, each with one lamp and two light switches, EDA software would create a netlist describing all of the cells on our chip—in this example, a collection of "and" and "or" cells—and the wires running between them.

During ***placement***, EDA software determines the location on the chip for each cell in the netlist. And during ***routing***, the software determines the routes for the wires that interconnect the cells in the circuit, as well as the wires that will run to the edges of the chip and contact the "pins" connecting the chip to the outside world. Placement and routing processes result in a detailed physical layout of the chip, precisely locating within the chip's boundary each of the components and the wires that interconnect them. This placement and routing process is the same for chips as simple as the five-cell light switch controller described above, and those as complex as a computer's microprocessor with hundreds of millions of cells. As the complexity of the chip being designed rises, the demands on the EDA software—in terms of speed, memory requirements, and the ability to change designs on the fly—also rise exponentially. Modern EDA software like that sold by Magma and Synopsys is extraordinarily complex, and is critical to the development of modern chips.

IV. THE PATENTS IN SUIT

The patents at issue in this case relate to four different parts of this EDA process. In order of the EDA process flow, they start with Magma's '328 patent, which claims a common data model for all of the EDA design software. From synthesis through placement and routing, each piece of design software (each is generally called a "tool") will use the same data model, without stopping to translate between tools.[1]

Magma's '745 and Synopsys's '508 patents relate to placement tools. As the cells are placed on the chip, certain regions may end up having more wires and cells than others, because a placement tool will not necessarily space all of the components perfectly. Areas with a cluster of cells and wires may be "congested," just as traffic is congested in certain areas of a city. And as with city traffic, congested regions in a chip lead to timing and interference problems. The '745 and '508 patents teach ways to better spread out chip components and relieve congestion.

Third, Magma's '116 and '093 patents relate to the placement and routing steps.[2] In the light switch example above, we might route a wire from the output of the "and" cell all the way across the chip to meet up with an output pin on the exterior of the chip. The chip in this example is so simple that a lengthy wire would be no problem. But in complex chips like today's microprocessors, lengthy wire routes can become a problem. Wires need to cross one another, leading to highway-interchange-like patterns of wires going up, down, and across, requiring more layers in the chip and more chip space to accommodate the ups and downs, and more wires inherently lead to more congestion. Ideally, the output of one cell should feed directly—or with only a very short wire—into the next cell, and the final output destined for a pin on the outside of the chip should exit

[1] The parties have agreed on the constructions of all the relevant terms in the '328 patent, and have listed them in a glossary that they propose be provided to the jury.

[2] The parties have agreed on the constructions of the relevant terms in the '093 patent, but because it is closely related to the '116 (the '093 is a continuation of the '116) in family and technology, Magma mentions it here.

a cell directly onto that pin, instead of being routed by wires across the chip. The '116 and '093 patents teach ways to achieve this "abutted-pin" design.

Finally, Synopsys's '733 and '501 patents relate to production testing of integrated circuits.[3] Because modern ICs are so complex, it would take far too long to fully test all the circuits on the chip after it is built to verify that all the circuits are functioning correctly. To simplify the testing of chips, EDA software designs into the chip what amount to test patterns, called "scan chains." Once the physical chip is built, it can be quickly and thoroughly tested by running the "scan chain" patterns. The '733 and '501 patents teach ways to design those scan chains into the chip.

V. CONSTRUCTION OF THE PATENT TERMS

The Federal Circuit's *en banc* decision in *Phillips v. AWH Corp.,* 415 F.3d 1303 (Fed. Cir. 2005), reaffirms the basic principles of claim construction, focusing on the language of the claims, the written description, and the prosecution history, in that order. *Id.* at 1312-17. Although expert testimony may be used if necessary to understand technical aspects of a patent, extrinsic evidence—in particular dictionary definitions—should be employed sparingly and only for confirmation. *Id.* at 1319. *Phillips* went on to re-emphasize that limitations appearing in the specification or in the preferred embodiment must not be read into the claims. *Id.* at 1323.

Phillips also highlighted ***why*** extrinsic evidence is less valuable than the patent and its prosecution history: because extrinsic evidence lends itself to being divorced from the patent and its claims. *Id.* at 1318-19. The Court criticized *Texas Digital Sys., Inc. v. Telegenix, Inc.*, 308 F.3d 1193 (Fed. Cir. 2002), since the *Texas Digital* methodology "placed too much reliance on extrinsic sources such as dictionaries, treatises, and

[3] Synopsys dedicated the '733 and '501 patents to the public shortly before the submission of these claim construction briefs. Because those patents remain in the case for purposes of Magma's antitrust and unfair competition counterclaims, Magma describes them briefly here.

encyclopedias and too little on intrinsic sources, in particular the specification and prosecution history." *Phillips*, 415 F.3d at 1320.

A. The Court Need Not Construe Terms That Are Sufficiently Clear To Be Understandable By A Lay Judge Or Juror

The Court need not construe simple words and phrases if they are sufficiently clear and can be readily understood by a lay judge or juror. *See Phillips*, 415 F.3d at 1314; *ASM Am., Inc. v. Genus, Inc.*, 260 F. Supp. 2d 827, 850 (N.D. Cal. 2002). Because there is nothing ambiguous or linguistically obscure about simple terms, they present little risk of jury confusion, and an instruction that each term should have its plain and ordinary meaning is sufficient. *See Lucent Techs., Inc. v. Newbridge Networks Corp.*, 168 F. Supp. 2d 181, 191 n.3 (D. Del. 2001).

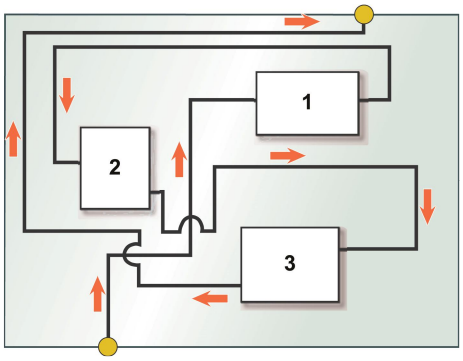
Because the claim language defines the scope of the claim, claim construction analysis must always center on the words of the claim. *See Teleflex, Inc. v. Ficosa N. Am., Corp.,* 299 F.3d 1313, 1324 (Fed. Cir. 2002). Those words are "generally given their ordinary and customary meaning," and the "ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, *i.e.*, as of the effective filing date of the patent application." *See Phillips*, 415 F.3d at 1313.

Courts agree that there is often no better way to define claim terms than to use the language of the claim itself. In *ASM America*, the court held that "there is no better way to define 'generally circular' than to simply say 'generally circular.'" 260 F. Supp. 2d at 850. And in *Applera Corp. v. Micromass UK Ltd.*, the court held that "to provide improved transmission of ions through said interchamber orifice" required no further construction, because the proper construction was "self-evident from the face of the claims." 186 F. Supp. 2d 487, 526 (D. Del. 2002); *See also*, *STMicroelectronics, Inc. v. Motorola Inc.*, 327 F. Supp. 2d 687, 698 (E.D. Tex. 2004) (declining to construe four claim terms, as each was "clear on its face"); *Lucent Techs. Inc.*, 168 F. Supp. 2d at 191

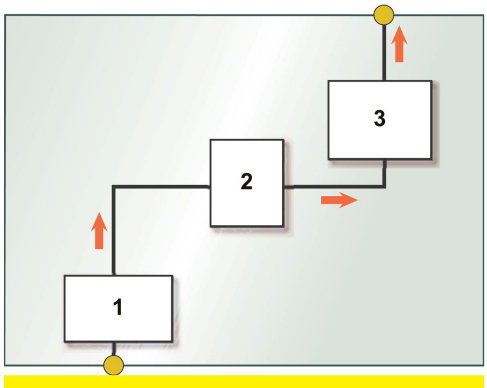
n.3 (terms were "self-explanatory" and required no construction). Even technical terms of art do not always need to be construed. *See UniRAM Tech., Inc. v. Monolithic Sys. Tech., Inc.*, No. C-04-1268, 2006 WL 825460, at *10 (N.D. Cal. March 30, 2006) (declining to construe "SRAM" because it "is a term well-known by persons of ordinary skill in the art.")

B. The '116 And '093 "Abutted-Pin" Patents

The '116 and '093 patents both address "abutted-pin hierarchical physical design" and are related: the '093 patent is a continuation of the '116. As mentioned above, the patents seek to optimize physical design by placing cells or blocks of cells near one another and near input and output pins of the chip, so that complex and lengthy wiring can be eliminated. For example, the following is a hypothetical chip design of a chip with three logic blocks, one input pin, and one output pin:



After attempting to improve the design with an abutted-pin approach as taught in the patents, the cells might be moved and rotated so that chip would look like this:



The operation of both chips is the same, but by eliminating unnecessary and complex wiring, the second design is simpler to fabricate, will take fewer layers of metal interconnections, and is less likely to have congestion problems.

The parties dispute the construction of only one term in the '116 patent, and they have agreed about all terms in the '093 patent.

1. "generating said physical design"

'116 Patent Claim Term (and claims)	Magma's Proposed Construction	Synopsys's Proposed Construction
generating said physical design (Claims 1-28)	**Plain meaning – no construction needed**	producing an improved physical design for the current integrated circuit

The term at issue in the '116 patent is "generating said physical design." Independent claim 1 illustrates the area of dispute. It teaches a "method of improving a physical design of a current integrated circuit, comprising the steps of," (a) receiving a netlist for that integrated circuit, (b) receiving some physical design information from a prior circuit, and (c) generating the physical design for the current IC based on the netlist and on the prior physical design.

What the preamble to independent claims 1 and 15 reveals—besides the antecedent for "said physical design"—is merely a goal of improving the circuit under examination. The jury needs no assistance in understanding what this claim teaches, or specifically, what element "(c)" of the claim means. It means just what it says: generating a physical design based on the netlist and the prior physical design information.

The claim requires no construction and should be given its plain and ordinary meaning. As in *ASM Am.,* 260 F. Supp. 2d at 850 ("no better way to define 'generally circular' than to simply say 'generally circular'"), or *Applera Corp.,* 186 F. Supp. 2d at

526 (construction "self-evident from the face of the claims"), "generating said physical design" means generating the physical design referred to in the preamble.

Synopsys's proposed construction improperly seeks to add limitations to the claim. Instead of allowing claim element (c) to mean what it says, Synopsys inserts the superfluous text "producing an improved physical design." First, "generating" does not need construction. And even if it did, "producing" as a substitute provides no clarification. Synopsys proposes removing and replacing a clear word that already has an ordinary meaning. This would not assist the jury.

Second, nothing in the claims mandates that the resulting design be "improved." Of course, that is the goal or the aspiration of the invention, but the patent can be practiced even if that goal is not achieved. The intrinsic evidence makes this clear. In discussing the reasons why it is desirable to feed more than one circuit's prior physical design into the decision-making process described by the claims, the specification states, "Thus, if physical design information 930 has information about several prior integrated circuits, the current integrated circuit is ***more likely to be optimized***." (Joint App., Ex. 19 ('116 Patent) at A-252, 9:33-35, emphasis added)[4]. That the circuit is more likely to be optimized under some conditions necessarily implies that it is less likely to be optimized under others, which in turn means that optimization is not possible in every instance. Magma agrees with Synopsys that the invention is useful to optimize a circuit, but "improvement" of any given circuit is not a requirement of the claim.

Third, the construction Synopsys proposes is unnecessarily confusing. As noted above, Magma agrees that the preamble must be read as part of independent claims 1 and 15. The preamble describes the goal of improving the physical design. But nothing in claim element (c) as drafted by the patentee suggests that any specific design must be

[4] Unless otherwise designated, all references to "Cooley Decl." refer to the supporting Declaration of Edmond S. Cooley, D.Eng., filed herewith and references to "Joint App., Ex. __" refer to the Joint Appendix of Intrinsic and Extrinsic Evidence, to be filed in conjunction with the parties respective *Markman* Reply briefs.

"improved" in order to satisfy element (c). Synopsys has simply extracted language from the preamble, recast it in different form and meaning, and inserted it into a claim element. This unnecessarily risks jury confusion over the substantial difference between "a method of improving" and "improved"; and it adds a limitation that the patentee clearly did not intend. There is no legitimate reason to rewrite the claim from one that defines an objective to one that requires an outcome.

C. The '745 Congestion Patent

There are two claim terms at issue in the '745 patent. Each is discussed in turn below.

1. "buckets"

'745 Patent Claim Term (and claims)	Magma's Proposed Construction	Synopsys's Proposed Construction
buckets (Claims 1-8)	a coarse, rectangular region within the chip's core area	rectangular, coarse placement region within the chip's core area

The disputed term "buckets" in the '745 patent refers to the regions into which a chip can be divided to study congestion. If the chip is viewed as a city map, some regions may be congested with traffic, while others flow freely. The '745 patent is focused on re-allocating resources within the chip in an effort to modify those congested regions, moving some of their traffic to the free-flowing areas. Before starting that process, though, the '745 teaches that the city map, the view of the chip from above, must first be divided into regions, or "buckets."

The dispute over "buckets" is limited to one issue: is a bucket a "placement region" (Synopsys's construction) or simply a "region" (Magma's construction) within the chip? The difference is consequential, since Synopsys wants to argue that buckets may only be formed after placement occurs. This is not a fair reading of the claim.

The specification does not define "buckets." In describing the preferred embodiment, the specification states: "More specifically, the core 400 where the cells are placed is divided into coarse placement regions called buckets 410 as shown in FIG. 4. Each bucket 410 is a small rectangular region within the core … A bucket 410 can accommodate about fifty average-sized standard cells." (Joint App., Ex. 8 ('745 Patent) at A-66, 6:47-54.) Thus the preferred embodiment uses the term bucket both as a "placement region" and as a "small rectangular region." But even if the preferred embodiment were clear, it would remain improper to import limitations from the specification into the claims, or to limit construction of a term to the preferred embodiment. *Phillips*, 415 F.3d at 1323.[5]

Neither the specification nor the prosecution history contains "words or expressions of manifest exclusion or restriction, representing a clear disavowal of claim scope" to show that the patentee clearly intended to limit the invention to "placement regions." *Teleflex,* 299 F.3d at 1327.

Independent claim 1 also says nothing to suggest that buckets can only be created after placement has happened. Instead, it calls for "grouping a plurality of cells in the design into a plurality of buckets." The claim goes on to require a congestion measure, and ***when routing*** a wire through a bucket, modifying that measure of congestion.[6] At some point, wires are placed and routed through the buckets. But this does not mean that the buckets must be defined ***during*** placing and routing. Synopsys is trying to create a limitation where none exists.

The Examiner's Notice of Allowability accords with Magma's construction. The Examiner found that no prior art taught, *inter alia*, "subdividing the chip area of a circuit

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[5] This includes reading limitations from the drawings into the claims. *See Gart v. Logitech, Inc.*, 254 F.3d 1334, 1342 (Fed. Cir. 2001).

[6] The preferred embodiment teaches generating the buckets in a first placement, but that approach is not mandatory.

design ***to be placed and routed*** into a coarse grid of buckets…" (Joint App., Ex. 36 ('745 Patent, Notice of Allowability) at A-624 ¶ 4, emphasis added.) Thus, the Examiner's view of the claim suggests that the division of the core into buckets takes place ***before*** placing and routing, not after.

The claim language is plain on its face, and the construction that best expresses its plain meaning, and is most consistent with the disclosed embodiments and with the applicant's and Examiner's understanding, is "a coarse, rectangular region within the chip's core area."

2. "congestion score"

'745 Patent Claim Term (and claims)	**Magma's Proposed Construction**	**Synopsys's Proposed Construction**
congestion score (Claims 1-8)	a ratio measure of routing resources	the ratio of routing resources used so far to the total routing resources available

The parties have a similar dispute over the proper construction of "congestion score" in the '745 patent. The "congestion score" measures the crowding of wires and cells within each bucket, and it is described in the '745 patent as a "ratio." In terms of automobile traffic, a highway might be thought of as 1%, 50% or 100% congested, or, alternatively, as 100%, 50% or 1% free-flowing. But regardless of how it is calculated, the percentage is a ratio used to measure congestion.

Magma's construction—"a ratio used to measure routing resources"—is consistent with all the embodiments disclosed in the patent and with the Examiner's understanding. Synopsys's, in contrast, would limit the term to the preferred embodiment, ignoring the other embodiments disclosed and claimed.

Synopsys proposes "the congestion score for a bucket is defined as the ratio of the routing resources used so far to the total routing resources available in the bucket." To continue the traffic analogy, Synopsys's definition is the number of lanes full of cars divided by the total number of lanes. It is true that the ***preferred embodiment*** calculates the congestion score in this manner. (Joint App., Ex. 8 ('745 Patent) at A-67, 8:33-36.)

But Synopsys's construction conflicts with the ***alternative embodiment*** disclosed in claim 2, which expressly defines the "congestion score" as "a ratio of a number of available wire routing spaces in a given layer of the bucket in a given direction to a total number of wire routing spaces…." In traffic terms, this is the reverse of the preferred embodiment's calculation—it is the number of ***empty*** lanes divided by the total number of lanes.[7]

As the *Phillips* court noted, the claims define the scope of the invention. *Phillips*, 415 F.3d at 1312. Claim 2's alternative embodiment proves that Synopsys's construction cannot be correct. *See RF Delaware, Inc. v. Pacific Keystone Techs, Inc.*, 326 F.3d 1255, 1265 (Fed. Cir. 2003) ("[C]ourts may not use the teaching of the specification to contradict the clear language of the claims.")

Moroever, claim differentiation would not permit a construction contradicted by a dependent claim: "Other claims of the patent in question, both asserted and unasserted, can also be valuable sources of enlightenment as to the meaning of a claim term." *Phillips*, 415 F.3d at 1314. Differences among claims are particularly important. "For example, the presence of a dependent claim that adds a particular limitation ***gives rise to a presumption that the limitation in question is not present in the independent claim***." *Id.* at 1314-15 (emphasis added).

[7] The preferred embodiment sees the glass as 50% full; claim 2 sees the same glass as 50% empty. But both measures are a ratio of how much water is in the glass.

The specification and claim 2 use different calculations to arrive at the "congestion score." The only coherent definition that can apply to the patent as a whole is necessarily broader: the congestion score is "a ratio measure of routing resources."

Magma's construction is also consistent with the definition used by the Examiner in the Notice of Allowability: "this congestion score (***ratio***) is then used to determine the spacing of the wires…" (Joint App., Ex. 36 ('745 patent, Notice of Allowability) at A-624, ¶ 4, emphasis added.)

The congestion score is just a ratio. In some instances, that ratio is the number of full lanes divided by the total number of lanes; in others, it is the number of empty lanes divided by the total. But in every instance, it is a ratio used to measure routing resources.

D. Synopsys's '508 Congestion Patent

The core problem with Synopsys's proposed constructions of the terms in the '508 patent is that Synopsys is trying to stretch a patent that provided an incremental improvement to outmoded technology (the "min-cut" system described below) to fit over modern "force directed" congestion-reduction technology. To do so, Synopsys is forced into strained positions, including reading the critical term "bin" out of the patent claims, arguing that plural terms are actually singular, and arguing that reducing congestion is not what the patent seeks to accomplish. Those arguments are not plausible. The patent amply describes Synopsys's invention. That invention, however, is not the force directed technology independently developed by Hans Eisenmann and Frank Johannes around the same time Magma filed its patent application. Synopsys should not be permitted to revise history to cover something it did not invent and to disrupt an industry that adopted the newer, superior technology.

A brief description of the differences between Synopsys's approach and the force directed approach helps illuminate the motivations for Synopsys's arguments and sheds light on how one of skill in the art interprets the claims of the '508 patent.

1. Congestion and the '508 Patent

As noted above, congestion—from too many cells or too many wires in too small an area—is undesirable. Since the tools that initially place components may not space them optimally, EDA software performs subsequent placement steps to reduce the congestion on the chip. The invention of the '508 patent is one technique for reducing congestion. As explained in the first line of the abstract of the patent, and in the first line of the summary of the invention: "This invention recognizes the ability of logic optimization ***to help placement relieve congestion***." (Joint App., Ex. 1 ('508 Patent) at A-6, 2:21-22.)

2. Congestion Algorithms – "ForceDirected"

Although there are a number of different techniques or mathematical algorithms available today for helping placement reduce congestion, they can be broken up broadly into two categories: (1) simulation-based algorithms and (2) partitioning-based algorithms. As explained in the textbook, *Algorithms for VLSI Physical Design Automation* ("Algorithms for VLSI"):[8]

> Simulation based algorithms simulate some natural phenomenon while partitioning based algorithms use partitioning for generating the placement.

(Joint App., Ex. 37 at A-629.)

The modern "force directed" approach to reducing congestion is a simulation-based algorithm:

> There are many problems in the natural world which resemble placement and packaging problems. Molecules and atoms arrange themselves in crystals, such that these crystals have minimum size and no residual strain. Herds of animals may move around, until each herd has enough space and it can maintain its predator-prey relationships with other animals in other herds. The simulation based placement algorithms simulate some of such natural processes or phenomena. There are three major algorithms in this class: simulated annealing,

[8] (Joint App., Ex. 37 at A-629**,** Naveed Sherwani, *Algorithms for VSLI Physical Design Automation*, 225 (Kluwer Academic Publishers 1999).)

> simulated evolution and force directed placement… [F]orce directed placement ***simulates a system of bodies attached by springs.***

(*Id*. at A-629-30, emphasis added.)

In the force directed approach, each logic cell can be thought of as being connected to its neighbors and to the edge of the chip by springs. A "heavier" cell (one likely to cause congestion problems) will naturally tend to pull away from its neighbors, reducing congestion. If it were replaced with a simpler, less congestion-inducing, and therefore "lighter" cell, it would move closer to its neighbors. The force directed algorithm, by modeling the entire chip as a series of spring forces, is able to find the best placement for each component without having to partition the chip. The computer power needed to create such a model for a complex chip is huge, making force directed placement practical only recently.

3. Congestion Algorithms—"Min-Cut"

In contrast, partitioning-based algorithms such as "min-cut" are simple: they repeatedly divide the chip into smaller and smaller partitions or "bins," and then address the congestion for each bin separately. These algorithms do not analyze the system as a whole, but instead identify individually congested bins and uses placement to reduce the congestion of the more congested bins (either by adjusting the placement within the bin, or moving components in a congested bin to a less congested bin). (Cooley Decl. at ¶ 11.) Referring back to the traffic analogy, "min-cut" is akin to using a detour to reroute traffic in one particular city block to adjust congestion, while force directed planning ignores artificial grid lines and involves more global planning of the street layout and street sizes.

4. The Force directed and Min-Cut Approaches

At the time Synopsys applied for the '508 patent in 1998, min-cut was the most widely-used placement algorithm. (Cooley Decl. at ¶ 13.) By 1998, min-cut, with all its limitations and in various incarnations, had been used by industry for over ten years. (Cooley Decl. at ¶ 14.) At that time, while companies like Synopsys were searching for

ways to improve min-cut, engineers, such as Hans Eisenmann and Frank Johannes from the Institute of Electronic Design Automation at the Technical University Munich were considering algorithms that took a completely different approach to placement.

At around the same time Synopsys filed its min-cut patent, Messrs. Eisenmann and Johannes were working on a possible force directed approach, and invented an innovative new mathematical algorithm for reducing congestion. In May of 1998, they presented their new force directed approach at the 35th Annual Conference on Design Automation (DAC)--the premier EDA trade show and conference. (Cooley Decl. at ¶ 15 and Cooley Decl. Ex. B (H. Eisenmann and F. M. Johannes, "Generic Global Placement and Floorplanning," in Proceedings of the 35th Design Automation Conference, pages 269-74 (1998)) (the seminal paper presenting the industry's modern force directed approach).) Nowhere does the '508 patent acknowledge force directed methodology generally or refer to the technology developed by Messrs. Eisenmann and Johannes. Instead, the '508 claims an incremental improvement to the then-popular partition-based algorithms. (Cooley Decl. at ¶¶ 16-17.)

5. The '508 Patent Is Aimed At Min-Cut Systems

Not only does the '508 patent never discuss the force directed approach or use any of the terminology traditionally used to describe the approach, the patent repeatedly discusses partitioning and bins, and focuses on how logic modification can reduce congestion within a bin or between bins. (Cooley Decl. at ¶ 17; *see also* Joint App., Ex. 1 at A-6, 2:21-22 ("This invention recognizes the ability of logic optimization to help placement relieve congestion.") and A-8, 5:1-39 (discussing logic modifications within and between bins).)

As explained in the patent:

> The present invention may be used in conjunction with an electronic design automation placement tool. In accordance with an exemplary embodiment of one such placement tool, at each stage in the cell placement, the cells are ***partitioned into a number of bins***.

(Joint App., Ex. 1 at A-7, 3:31-35, emphasis added.)

The patent goes on to describe "logic modifications." The basic concept behind logic modifications is that certain collections of logic gates are equivalent to others. For instance, as noted above, we might be able to achieve the goal of controlling lamps in a house with a variety of different combinations of AND and OR gates, and each different combination would have a different impact on congestion. Figures 4, 5, and 6 in the '508 patent illustrate logic circuits that have the same function, but may have different effects on congestion.

The patent describes improving a congested "bin" by (1) reducing the total number of logic gates within that bin (*see* Joint App., Ex. 1 at A-4 Figs. 4a and 4b and Joint App., Ex. 1 at A-4, 5:3-12), (2) moving gates from a congested bin to a less congested bin (*see id.* at A-4, Figs. 5a and 5b and A-8, 5:13-25), or (3) dividing the inputs to a logic circuit so that at least some parts of the circuit can be moved to more free-flowing areas (*see id.* at A-4, Figs. 6a and 6b and A-8, 5:26-33.). The central invention, however, remains simple: by exploring different ways to perform the same logic operations, it may be possible to reduce congestion in particular bins on the chip.[9]

This focus on congested bins, and on efforts to exchange one logic circuit for another to shift congested areas from one bin to another, are all core to the min-cut approach. Force directed algorithms, by contrast, do not use bins or logic modifications; for Synopsys to argue that its patent applies to spring simulation force directed systems simply makes no sense.

[9] For example, a circuit designed to multiply two numbers could be built several ways. The most obvious is the multiplication taught in elementary school—15 times 3 is 45, with a notation to "carry the 1." But the circuit could also start at 0, and add 15 to the total 3 times. It might be faster, and simpler logically, to use elementary school multiplication, but the two approaches achieve the same result, and would be built with very different logic gates, making their impacts on congestion very different.

6. The '508 Patent's Improvement To The Min-Cut System Was Rejected By Industry

Shortly after Synopsys applied for the '508 patent, the EDA industry began shifting to the more complex—but superior in application—force directed algorithms to place cells and address congestion.

Recognizing this, and even though its claims had finally been allowed, the '508 patent applicant amended the preamble of all of the independent claims in its '508 application and stated that the amendments would "account for the possibility of performing the present invention using only a single bin"[10] (*i.e.*, a force directed approach in which the entire circuit could be considered a single "bin"). The amendments were entered, but there is nothing in the original specification, the patent as-filed, that describes a chip with a single bin (and Synopsys cited no support to the examiner when it filed that amendment). Its amendments were therefore improper new matter and cannot be used to change the original disclosure. "[O]ne can not interpret a claim to be broader than what is contained in the specification and claims as filed." *See Tandon Corp. v. U.S. International Trade Com.*, 831 F.2d 1017, 1024 (Fed. Cir. 1987). This requirement "prevents applicants from using the amendment process to update their disclosures (claims or specifications) during their pendency before the patent office. Otherwise applicants could add new matter to their disclosures and date them back to their original filing date…" *Chiron Corp. v. Genentech, Inc.*, 363 F.3d 1247, 1255 (Fed. Cir. 2004); *see also TurboCare Div. of Demag Delaval Turbomachinery Corp. v. General Elec. Co.*, 264 F.3d 1111, 1118 (Fed. Cir. 2001) ("When the applicant adds a claim or otherwise amends his specification after the original filing date…the new claims or other added material must find support in the original specification.")

[10] Joint App., Ex. 2 at A-14.

For the purposes of claim construction, Synopsys's patent claims mean what they say: they teach partitioning the chip into bins, and using logic modifications to move some congestion to free-flowing bins. (*See* Cooley Decl. at ¶ 20.)

7. "Bin" Means "Rectangular (or Square) Portion Of An Integrated Circuit Bounded By Gridlines"

'508 Patent Claim Term (and claims)	Magma's Proposed Construction	Synopsys's Proposed Construction
Bin (Claims 1-15, 17, 18)	a rectangular (or square) portion of an integrated circuit bounded by gridlines	a region

Because bins were such an elemental part of the then-popular min-cut system, the '508 inventors felt no need to define the term. Extrinsic evidence is thus appropriate. *Digital Biometrics,* 149 F.3d at 1344 (Fed. Cir. 1998) (if, after consideration of intrinsic evidence there remains doubt as to the exact meaning, consideration of extrinsic evidence may be necessary); *Phillips,* 415 F.3d at 1319 (Fed. Cir. 2005) (extrinsic evidence can help the court determine what a person of ordinary skill in the art would understand claim terms to mean). One of ordinary skill in the art at the time would define a bin as a "rectangular (or square) portion of an integrated circuit bounded by gridlines." (Cooley Decl. at ¶ 9).[11] Synopsys cannot legitimately dispute this. The inventors of the '508—persons of skill in the art[12]—themselves, used the "bins" in one of their other placement patent--U.S. Patent No. 6,442,743 ("'743 patent"). *See Ampex Corp. v. Eastman Kodak Co*., No. Civ. A. 04-1373 KAJ, 2006 WL 3042144 at *9 (D. Del. October 26, 2006) (construing "video image," and using company's other patents for clarification of the term). In the '743 patent, the inventors depict bins this way:

[11] The inventors' belated definition of bin in an amendment to the patent was unsupported by the original disclosure and is therefore of no weight.

[12] *Phillips,* 415 F.3d at 1313 (noting the "well-settled understanding that inventors are typically persons skilled in the field of the invention"). Indeed, Profs. Pileggi and Malik teach university-level integrated circuit design and two other inventors are currently employed by Synopsys for integrated circuit design.

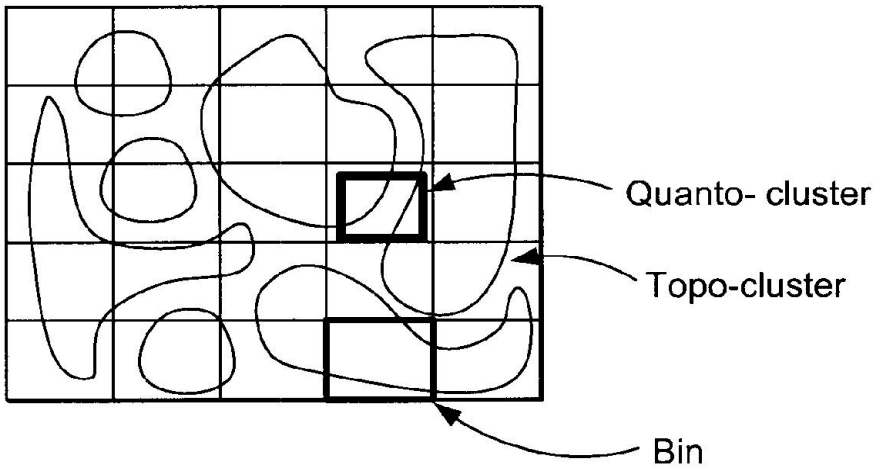

FIG. 3

As the inventors show in Figure 3 and discuss in the text of the '743 patent, a "bin" is a rectangle (or square) bounded by gridlines. (Joint App., Ex. 27 at A-482.) "Bins" are generally rectangular because their purpose is to divide the circuit into similarly sized areas through the use of a grid. In Figure 3, for instance, the grid consists of 25 bins (5 rows of 5).

This definition of "bin" is confirmed in publications by those of ordinary skill in the art. *See*, *e.g.*, "Application-Specific Integrated Circuits," Michael John Sebastian Smith, 1997, p. 882-885 (Joint App., Ex. 33 at A-560-63) (showing a grid pattern of bins in Fig. 16.24); Chang, *et al.*, "Physical Hierarchy Generation with Routing Congestion Control," ISPD 2002 (Joint App., Ex. 25 at A-462) (showing a grid pattern of bins in Figure 2); and U.S. Patent No. 5,847,965 at col. 4:55-56 (Joint App., Ex. 26 at A-475) (noting that "[t]he core area is partitioned into a two-dimensional array of grids. The grids, also known as buckets or bins...").

And this definition of "bin" is also supported by expert opinion. (Cooley Decl. at ¶¶ 8-12.) Indeed, the very name reflects the process by which the bins are created: that

is, by sequentially dividing or "cutting" the cells of a chip into smaller and smaller bins using gridlines. (Cooley Decl. at ¶ 10.)

Synopsys's proposed construction "a region," is transparently aimed at reading the limitation "bin" out of the claims so they could be read to cover systems that do not use partitioning. In fact, the Synopsys inventors themselves specifically distinguish between "bins" and "regions" in their '743 patent, using the term "region" much more broadly to cover a "window" of multiple bins. (Joint App., Ex. 27 at A-492, 6:59-64.) By conflating bins with regions, Synopsys hopes to read out the concept of bins -- and thus partitioning -- from the claims, enabling it to argue that its min-cut patent should apply to modern technology. In interpreting claim terms, however, this Court "must give each claim term the respect that it is due." *Pause Tech. LLC v. TiVo Inc.,* 419 F.3d 1326, 1334 (Fed. Cir. 2005). "All limitations in a claim must be considered meaningful," and it is clear legal error to read out limitations from a claim. *See Lantech, Inc. v. Keip Mach. Co.,* 32 F.3d 542, 546-47 (Fed. Cir. 1994); *see also Optical Disc Corp. v. Del Mar Avionics*, 208 F.3d 1324, 1337 (Fed. Cir. 2000) (discussing *Tronzo v. Biomet* 156 F.3d 1154 (Fed. Cir. 1998), in which the court rejected expert testimony that "any shape would be equivalent to the recited conical limitation, reemphasizing that "such a result is impermissible … because it would write the 'generally conical outer surface' limitation out of the claims."). Consequently, this Court should construe the term "bin" to mean something more than simply "a region;" specifically, it should be construed to mean, "a rectangular (or square) portion of an integrated circuit bounded by gridlines."

8. "Bins" Means "More Than One Bin"

'508 Patent Claim Term (and claims)	Magma's Proposed Construction	Synopsys's Proposed Construction
Bins (Claims 1-18)	more than one bin	one or more regions

Synopsys continues its attempt to read out partitioning and bins by arguing that the plural word "bins" means just one bin. This argument goes hand-in-hand with Synopsys' argument that "bin" means "region." The combinations of the arguments would completely eviscerate the claim limitation "bins" as any chip layout, whether or not partitioned into bins, would meet the claim limitations, because all layouts have at least one region. It is not coincidental that modern force directed algorithms use no bins, and the only plausible way to infringe would be to call the entire chip one large "region."

"Bins" is the plural of bin, and the actual words of the claim are controlling in claim construction. *Digital Biometrics, Inc. v. Identix, Inc*., 149 F.3d 1335, 1344 (Fed. Cir. 1998). Here, the words of the claim are clear, and they are plural. *See ASM America, Inc. v. Genus, Inc.,* 260 F. Supp. 2d 827, 850 (N.D. Cal. Nov. 14, 2002) ("generally circular" meant generally circular).

The specification accords with this construction. *See, e.g., Leggett & Platt, Inc. v. Hickory Springs Mfg. Co.,* 285 F.3d 1353, 1357 (Fed. Cir. 2002) ("At the outset, the claim recites 'support wires' in the plural, thus requiring more than one welded 'support wire'" (emphasis added)). The '508 patent discloses only one method for calculating congestion: the number of pins in a bin divided by routable area of the bin. (Joint App., Ex. 1 ('508 Patent) at A-7, 4:53-55.) If bins meant just one bin (or one region), that congestion measure would be meaningless. (Cooley Decl. at ¶ 18.) In traffic terms, knowing that there are 10,000 cars on 1200 miles of road in Wilmington would tell us nothing about ***where*** traffic is congested—it is the number of cars in each small rectangular area on the map that is relevant.

Similarly, the patent classifies logic modifications as either "inter-bin" or "intra-bin"—some equivalent logic can inherently reduce congestion in its own bin, while other equivalent logic, such as division of inputs to a circuit, enables the designer to spread congestion into other, more free-flowing bins. (Joint App., Ex. 1 at A-8, at 5:1-44.) Neither would make sense if the inventors had contemplated having a single bin.

The term hardly needs construction; the plain and ordinary meaning of a plural word is clear. Magma proposes its construction only to highlight Synopsys's attempt to read out the plural.

9. "Selected Bins" Means "More Than One Bin Selected Based On Congestion"

'508 Patent Claim Term (and claims)	Magma's Proposed Construction	Synopsys's Proposed Construction
selected bins (Claims 1-18)	more than one bin selected based on congestion	one or more selected regions

Again, Synopsys tries to read out of the patent both bins, and how a bin is selected. The specification states that congested bins are targeted or "selected" for logic modifications ***to reduce congestion***. (Joint App., Ex. 1 at A-7, 3:53-56) ("logic synthesis is used to aid placement to achieve both acceptable delays and congestion, by making circuit modifications that increase the timing slack in the congested parts"); (*Id.* at A-7, 4:54-55) ("Identification of congested bins [] is done using the congestion estimates for each bin."). And the third step shown in Figure 2 is the identification of congested circuits "for placement moves to relieve congestion." (*Id.* at A-7, 3:56). Thus, "selected bins" are those selected for congestion purposes.

There is no other description in the specification or the file history about how bins could be selected, and no indication that the meaning of "selected bins" varies from claim to claim. *Fin Control Systems Pty, Ltd. v. OAM, Inc.*, 265 F.3d 1311, 1318 (Fed. Cir. 2001) (presumption that same terms appearing in different portions of claims should be given same meaning unless it is clear from the specification and prosecution history that terms have different meanings at different portions of the claims)*; see also Phillips*, 415 F.3d at 1314 ("claim terms are normally used consistently throughout the patent").

The ineluctable conclusion is that "selected bins" refers to bins "selected based on congestion."[13] It is not surprising that under Synopsys's construction, **any** layout might meet the limitation "selected region," because the "region" could mean the entire chip. Synopsys's proposal is yet another brazen attempt to stretch the '508 patent over modern force directed technology.

10. "In An Attempt To Improve Congestion By Taking Advantage Of The Logic Modifications / To Allow Congestion Of The Placement To Be Improved / Reducing Constraints On A Subsequent Placement Step" All Mean"…With The Purpose Of Reducing Congestion…"

'508 Patent Claim Term (and claims)	Magma's Proposed Construction	Synopsys's Proposed Construction
in an attempt to improve congestion by taking advantage of the logic modifications (Claims 2-11, 13, 14)	with the purpose of reducing congestion by taking advantage of more than one logic modification	to relieve congestion where opportunities are provided by logic modifications.
to allow congestion of the placement to be improved	with the purpose of reducing congestion of the placement	to provide opportunities for placement to improve congestion

[13] In addition, "selected" bins must mean "selected based on congestion" because claims 17 and 18 would otherwise not comply with section 112, second paragraph 35 U.S.C. § 112 and would be invalid. *Acacia Media Technologies Corp. v. New Destiny Internet Group*, 405 F.Supp.2d 1127, 1138 (N.D. Cal. 2005). Claims 17 and 18 recite an apparatus having a "means for calculating congestion" and a "means for … performing logic modifications within selected bins…". The term "selected" in "selected bins" is ambiguous because the claim does not indicate how the bins are selected and also because the claim does not explicitly recite the use of the calculated congestions for anything. But the specification describes that the calculated congestion is used to identify congestion bins. (Joint App., Ex. 1 at A-7, 4:53-55.) Thus, for claims 17 and 18 to not be indefinite, "selected bins" must mean selected "based on congestion." This construction is proper because it is supported by the specification and, in fact, is the only logical interpretation of the term, given the description in the specification and the language of the claims. *Nazomi Communications, Inc. v. ARM Holdings, PLC*, 403 F.3d 1364, 1369 (Fed. Cir. 2005) (assessments of validity can and should be made to resolve claim construction when, after applying all the resources of construction, the claim term remains ambiguous); *Phillips v. AWH Corp.,* 415 F.3d 1303, 1327 (Fed. Cir. 2005) (claims can be construed to preserve their validity where the proposed claim construction is 'practicable,' is based on sound claim construction principles, and does not revise or ignore the explicit language of the claims).

'508 Patent Claim Term (and claims)	Magma's Proposed Construction	Synopsys's Proposed Construction
(Claims 1-11, 15, 17)		
reducing constraints on a subsequent placement step (Claims 12-14, 16, 18)	reducing more than one constraint on a subsequent placement step with the purpose of reducing congestion during the subsequent placement step	reducing one or more constraints on a subsequent placement step

These terms are grouped together because each is performed to reduce congestion. The first two terms explicitly acknowledge this—they "attempt to improve congestion" and "allow congestion…to be improved," respectively.

The third, "reducing constraints on a subsequent placement step," means "reducing more than one constraint on a subsequent placement step with the purpose of reducing congestion during the subsequent placement step," because that purpose is manifest in the intrinsic evidence.

a. "Constraints" is plural, and does not mean "one or more"

First, Synopsys's argument for the singular of "constraints" is undone by the claim language itself. As with bins, above, Synopsys cannot simply re-draft the claims now to make plural words singular. "Constraints" means more than one.[14]

b. The intrinsic evidence requires the purpose be to reduce congestion

Second, the inventors explicitly defined their invention as one to reduce congestion. The word "congestion" appears 56 times in the nine pages of the '508 patent, (Cooley Decl. at ¶ 24), and the intrinsic evidence is replete with references defining the invention as relieving or reducing congestion:[15]

[14] In addition, ***every time*** the word "constraint" is used in the specification, it is plural. (Cooley Decl. at ¶ 22.)

[15] Each of the claims also includes a step of calculating congestion. If the claimed invention were designed to reduce congestion, there would be no reason to calculate it.

> ***This invention*** recognizes the ability of logic optimizations to help placement ***relieve congestion***. (Joint App., Ex. 1 at A-6, 2:21-22, emphasis added.)
>
> ***This invention will*** significantly reduce, if not eliminate, the iterations needed by considering not only the impact of interconnect during logic optimization of area/timing, but also at the same time *doing logic optimizations to* ***help placement relieve congestion*** and thus generate a circuit that is easily routable. (Joint App., Ex. 1 at A-8, 6:30-35, emphasis added.)
>
> Rather, ***the approach of the present invention*** is to first reduce signal delays using conventional logic optimization techniques. This reduction in the signal delays provides additional slack that *can then be used by a subsequent placement step* ***to relieve congestion***. (Joint App., Ex. 23 (Response) at A-427, emphasis added.)
>
> *In the* ***present invention, congestion is addressed*** *through logic modification*. (*Id.* at A-426)

Under settled case law, the inventors' description of what they invented is limiting. Here, their invention's goal is to reduce congestion. *See Scimed Life Systems, Inc., v. Advanced Cardiovascular Systems, Inc*., 242 F.3d 1337, 1343 (Fed. Cir. 2001) ("the characterization of the coaxial configuration as part of the "present invention" is strong evidence that the claims should not be read to encompass the opposite structure."); *Watts v. XL Systems, Inc*., 232 F.3d 877, 883 (Fed. Cir. 2000) ("the specification actually limits the invention to structures that utilize misaligned taper angles").

The Examiner's understanding of the invention accords with that of the inventors: "there is no teaching [in the prior art] of specifically carrying out logic optimization ***in order to reduce congestion***." (Joint App., Ex. 39 ('508 Notice of Allowability) at A-640, emphasis added.)

In short, when the patent teaches logic modifications, it does so for the purpose of reducing congestion. *Renishaw*, 158 F.3d at 1250 (Fed. Cir. 1988) (The construction that aligns with the patent's description of the invention is the correct construction.)

c. The inventors disclaimed purposes other than reducing congestion

Third, long before the '508 patent, logic modification had been performed to improve timing. (Joint App., Ex. 1 at A-7, at 3:65 – 4:l.) The '508 patent's inventors claimed to be the first to realize that those timing improvements could be parlayed into congestion improvements. (*Id.* at A-7, 4:1-7.) But because logic modifications for the purpose of improving timing were well-known in the prior art, the '508 patent is limited to the novel feature of the invention: reducing congestion. *See O.I. Corp. v. Tekmar Co.*, 115 F.3d 1576, 1581 (Fed. Cir. 1997) (limiting the scope of the patent when the written description "expressly distinguishe[d] over prior art passages by stating that those passages are generally smooth-walled."); *Scimed Life Systems, Inc.*, 242 F.3d at1343 (Fed. Cir. 2001) ("Thus, the SciMed patents distinguish the prior art on the basis of the use of dual lumens and point out the advantages of the coaxial lumens used in the catheters that are the subjects of the SciMed patents. That discussion in the written description supports the district court's conclusion that the claims should not be read so broadly as to encompass the distinguished prior art structure.")

This limited claim scope was acknowledged by the inventors during prosecution. For example, the '508 patent notes:

> The ***traditional role of logic synthesis*** has been to identify areas of the circuit which have negative ***timing*** slack and then modify the circuit so as to fix this problem. (Joint App., Ex. 1 at A-7, 3:50-52, emphasis added.)
>
> A ***distinguishing feature*** of [the patent's] methodology is that it not only uses the placement information for interconnection delay/area estimates during logic optimization, but also uses logic optimization to aid the physical placement steps by providing support to placement ***so that the congestion of the circuit is improved***. (*Id.* at A-6, 2:28-33, emphasis added.)

Synopsys's proposed construction collapses to "doing something to somehow improve the circuit at some point during placement." That interpretation would be convenient for its infringement analysis, but it lacks any support in the intrinsic evidence

or the claims. The goal of the patent was to reduce congestion, (Cooley Decl. at ¶ 20) and Synopsys cannot read that out of the claims.

11. "Limits" Means "More Than One Bound"

'508 Patent Claim Term (and claims)	Magma's Proposed Construction	Synopsys's Proposed Construction
Limits (Claims 1-18)	More than one upper bound	upper bounds

Once more, Synopsys tries to re-define a plural word as singular. For the same reasons discussed above "limits" means more than one.[16] Had Synopsys wanted to claim a single bound, it could have. It did not. The term can be construed by its plain and ordinary meaning. Magma proposes a construction merely to highlight Synopsys's attempt to read out the plural.

12. Mean-Plus-Function Clauses (Claims 17 and 18)

The parties agree that claims 17 and 18 are means-plus-function claims. The parties disagree about how the claim terms define the function.

The first step in construing a means-plus-function claim limitation is to define the function of the claim limitation. The function is important because it limits how the "means" are to be used. *Roche Diagnostisc Corp. v. Apex Biotechnology Corp*., No. 1:04 CV 00358 LJM, 2005 WL 2363068, at *12 (S.D. Ind. 2005) ("the functional recitations contained in the pending claims are entitled to be given 'patentable weight' and to be considered as defining Applicants [sic] invention in full conformance with 35 USC [sic].")

The next step is to identify in the specification the corresponding structure for the function. *Golight Inc. v. Wal-Mart Stores, Inc.,* 355 F.3d 1327, 1333-4 (Fed. Cir. 2004). The '508 patent, and specifically claims 17 and 18, discloses a computer for performing

[16] And every time the word "limit" is used in the specification, it is used as the plural. (Cooley Decl. at ¶ 23.)

various algorithms. (Joint App., Ex. 1 ('508 Patent) at A-5, Fig. 7 and A-8, 6:3-23.) Corresponding structure for such claims is the special purpose computer programmed to perform the disclosed algorithm, instead of the computer itself. *WMS Gaming, Inc. v. International Game Technology*, 184 F.3d 1339, 1349 (Fed. Cir. 1999) ("In a means-plus-function claim in which the disclosed structure is a computer, or microprocessor, programmed to carry out an algorithm, the disclosed structure is not the general purpose computer, but rather the special purpose computer programmed to perform the disclosed algorithm"); s*ee also, Harris Corp. v. Ericsson, Inc*., 417 F.3d 1241, 1249 (Fed. Cir. 2005); *ABB Automation, Inc. v. Schlumberger Resource Management Services, Inc*., No. Civ.A. 01-077-SLR, 2003 WL 21034979, at *1 (D. Del. May 6, 2003).

The relevant functional elements and the corresponding structure for each of the disputed elements of claims 17 and 18 are as follows.

13. Means For Calculating Congestion Of The Initial Placement

'508 Patent Claim Term (and claims)	Magma's Proposed Construction	Synopsys's Proposed Construction
Means for calculating congestion of the initial placement (Claims 17, 18)	Construction of this phrase is governed by 35 U.S.C. § 112, ¶ 6. The claimed function is "calculating congestion of the initial placement." The corresponding structure is a computer performing: ○ calculating the total number of pins in the bin divided by the total routable area in the bin.	Construction of this phrase is governed by 35 U.S.C. § 112, ¶ 6. The claimed function is "calculating congestion of the initial placement." The corresponding structure is a computer performing: ○ calculating congestion for the initial placement using interconnection models for interconnects between bins or within bins; or ○ calculating congestion for the initial placement in accordance with an algorithm that calculates the total number of pins in the bin divided by the total routable area in the bin.

The parties agree that the claimed function is "calculating congestion of the initial placement." The parties' dispute is over the corresponding structure.

The only algorithm disclosed by the '508 patent is "calculating as the total number of pins in the bin divided by the total routable area in the bin." The patent is thus limited to that algorithm. (Joint App., Ex. 1 at A-7, 4:62-63); *Valmont Indus., Inc. v. Reinke Mfg. Co.*, 983 F.2d 1039, 1042 (Fed. Cir. 1993) (section 112, ¶ 6, permits the use of means-plus-function language in claims, but with the proviso that the claims are limited to the structure, material, or acts disclosed in the specification and their equivalents). Synopsys apparently agrees that this is the structure disclosed, as the second bullet point in Synopsys's proposal essentially tracks the specification's language.

Synopsys's first bullet point is improper, for these disclosure points to a class of models and does not specify any corresponding structure act or algorithm. *WMS Gaming*, 184 F.3d at 1349 ("the disclosed structure is … the special purpose computer programmed to perform the disclosed algorithm").

The only algorithm disclosed in the patent is "calculating the total number of pins in the bin divided by the total routable area in the bin." That is the corresponding structure.

14. Means For Performing An Initial Placement Of Integrated Circuit Elements Within Bins On The Design Layout

'508 Patent Claim Terms (and claims)	Magma's Proposed Construction	Synopsys's Proposed Construction
Means for performing an initial placement of integrated circuit elements within bins on the design layout (Claim 17)	Construction of this phrase is governed by 35 U.S.C. § 112, ¶ 6. The claimed function is "performing an initial placement of integrated circuit elements within bins on the design layout." The corresponding structure is: ○ [No corresponding structure is disclosed.]	Construction of this phrase is governed by 35 U.S.C. § 112, ¶ 6. The claimed function is "performing an initial placement of integrated circuit elements within bins on the design layout." The corresponding structure is: ○ placing cells in one or more regions using a placement tool that partitions cells into one or more regions at each stage of the placement; and ○ placing cells in accordance with a placement algorithm that is limited by the topology of the circuit.

Again, the parties agree about the function, but disagree about the structure—for there is no structure disclosed.

The '508 patent provides no algorithm for "performing an initial placement…within bins." The specification refers in general terms to a "placement tool," but it does not disclose any algorithm—and a specific description of the algorithm with which to program the computer is required. *WMS Gaming*, 184 F.3d at 1349 ("the disclosed structure is … the special purpose computer programmed to perform the disclosed algorithm"). Any number of algorithms could be a "placement tool," but the patent does not describe or identify even one.

Accordingly, this term should be 'construed' as lacking corresponding structure.

VI. CONCLUSION

Synopsys's strategy for claim construction speaks volumes. With only three exceptions (and then, on relatively minor points), it agrees that the Magma patents mean what they say. But then it turns an about-face, arguing for term after term that its own congestion patent *doesn't* mean what it says – that instead, it was aimed at technology years behind its time. Plurals are not singular, a "bin" is not an entire chip, and partitioning is not force directed modeling. Synopsys's efforts to redraft a 1998 patent to apply to today's technology should be rejected.

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DATED: November 3, 2006

CERTIFICATE OF SERVICE

I hereby certify that on November 3, 2006, I electronically filed with the Clerk of Court MAGMA DESIGN AUTOMATION'S OPENING MARKMAN BRIEF using CM/ECF which will send electronic notification of such filing(s) to the following Delaware counsel. In addition, the filing will also be sent via hand delivery:

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